Session 33 Overview

Mobile TV

Chair: Bud Taddiken, Microtune, Plano, TX

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TV on a mobile phone is not new. Analog TV tuners have been used in mobile phones in several countries over the years. However, the technology never took off because of the power and performance penalties inherent to analog TV broadcasting and receivers. Digital broadcasting technologies such as DVB-H, DMB, ISDB-T, and MediaFLO solve these technical problems. In a recent Credit Suisse First Boston forecast[1], it is estimated that 150M handsets per year will ship with digital TV reception capability by 2009 representing a new $1B opportunity for semiconductor manufacturers and many times that for handset manufacturers and mobile phone operators. In some countries these services are already commercially available today while many other countries are completing field trials and preparing for commercial introduction during 2006. The first six presentations in this session represent a snapshot of the recent advances in tuner integrated circuits for all of these mobile digital TV broadcasting technologies.

For the first time ever, a single chip DVB-H tuner is presented in this session. In fact, the first three papers all share this world's first. All three feature dual-band support for both European DVB-H requirements in the UHF frequency spectrum and US DVB-H requirements in the L-Band frequency spectrum. Papers 33.1 and 33.2 accomplish this using CMOS technology, while Paper 33.3 uses a SiGe BiCMOS process. The CMOS chips show smaller die size than that of the SiGe BiCMOS implementation, but the SiGe BiCMOS IC achieves better noise figure performance.

Paper 33.4 describes the world's first tuner IC for MediaFLO. Unlike the DVB-H tuners, it only operates in a narrow frequency range of 698MHz to 746MHz, but it has an extremely low noise figure of 2.6dB, consumes a mere 160mW, and has the smallest die area of any of the other tuners presented in this session.

The last two tuner papers in this session address DMB implementations. In addition to T-DMB operation in VHF Band-III and L-band, Paper 33.5 also demonstrates ISDB-T 1- and 3-segment operation in the VHF and UHF bands. Power consumption is only 100mW in the UHF band. This is the lowest continuous power of all the tuners in this session, and this is critical because DMB and ISDB-T are not able to take advantage of the power-saving feature of DVB-H known as time-slicing. The tuner presented in Paper 33.6 supports the S-DMB system. The previous five papers in this session are terrestrial tuners, but this one is for satellite reception of mobile digital TV. As such, it features the lowest noise figure of any of the six tuners presented in this session.

Finally, Paper 33.7 demonstrates a fully integrated frequency synthesizer for a DBS satellite tuner-demodulator SoC. With 0.3mm^2, it has much smaller die area than previous designs yet requires the fewest off-chip components.

33.1 A 0.18µm CMOS Dual-Band Direct-Conversion DVB-H Receiver **1:30 PM**

I. Vassiliou, Athena Semiconductors, Athens-Alimos, Greece

A 0.18µm CMOS direct-conversion dual-band DVB-H receiver occupies 9.7mm^2 and achieves a 4dB/5dB NF at UHF/L-band, eliminating the need for an external LNA. By using a fractional-N synthesizer, the 470 to 890MHz and 1.4 to 1.8GHz bands are supported while achieving an integrated phase noise of <–41dBc. 6th-order LPF support channel bandwidths from 4 to 10 MHz. The overall power consumption is 295mW/280mW for continuous operation in the UHF/L-Band, respectively.

33.2 A Multi-Band Multi-Mode CMOS Direct-Conversion DVBH Tuner **2:00 PM**

Y-J. Kim, Samsung, Yongin-City, Korea

A direct-conversion tuner is fabricated in a 0.18µm CMOS process. The vertical BJT is adopted to minimize the effects of 1/f noise. The tuner has a NF of 4.5dB (5dB), IIP3 of -5dBm (-6dBm), IIP2 of >40dBm, sensitivity of -89dBm (-88.5dBm) for 16-QAM CR $^1/_2$, and draws 66mA (74mA) from a 2.8V for UHF (USA L-Band).

33.3 Dual-Band Single-Ended-Input Direct-Conversion DVB-H Receiver **2:30 PM**

M. Womac, Microtune, Plano, TX

A 340mW single-chip direct-conversion tuner with single-ended input for UHF and L-band DVB-H is fabricated in a 0.35µm BiCMOS process. Included are 3 parallel LNAs, 2 I/Q mixers, 7th-order baseband filters, a fractional-N synthesizer, and dc-offset circuits. The NF is <3.6dB at maximum gain of >80dB, sensitivity is <-88dBm for 16-QAM CR 2/3, gain range is >60dB, IIP3 is >4dBm, IIP2 is >27dBm, die area is 12.25mm^2, and supply voltage is 2.7V.

33.4 A Dual-Channel Direct-Conversion CMOS Receiver for Mobile Multimedia Broadcasting **3:15 PM**

Y. Xu, Qualcomm, San Diego, CA

A 0.25µm CMOS receiver circuit that operates from 698MHz to 746MHz, a spectrum allocated by the FCC for advanced mobile services for multimedia applications, is presented. The receiver supports an OFDM physical layer with modulation ranging from BPSK for pilot carriers to 16-QAM for high-rate data carriers. The RX has a NF of 2.6dB and an out-of-band IIP3 of -5.5dBm. It occupies 7mm^2 and draws 61mA from a 2.6V supply.

33.5 A 100mW Dual-Band CMOS Mobile-TV Tuner IC for T-DMB/DAB and ISDB-T **3:45 PM**

B-K. Kim, Integrant Technologies, Seongnam, Korea

A 0.18µm CMOS dual-band low-IF mobile-TV tuner IC for T-DMB/DAB that supports Band-III and L-Band is presented. By modifying a few metal and via masks, the IC can support VHF and UHF bands for ISDB-T partial reception. The chip meets all the specifications of both applications with a sensitivity of <-98dBm while consuming 100mW from a 1.8V supply and occupying 3.4×3.3mm^2.

33.6 A 1.8dB NF 112mW Single-Chip Diversity Tuner for 2.6GHz S-DMB Applications **4:15 PM**

M-W. Hwang, FCI, Seongnam, Korea and KAIST, Daejeon, Korea

The fully-monolithic diversity 2.6GHz S-DMB tuner IC features a NF of <1.8dB, a path isolation of over 25dB, a DR of over 100dB with <4dB path gain mismatch and a power consumption of 112mW. This IC is implemented in a 0.25µm SiGe BiCMOS process. The chip is verified in S-DMB systems using several commercially available S-DMB demodulator chips.

33.7 A sub-1.5°$_{rms}$ Phase-Noise Ring-Oscillator-Based Frequency Synthesizer for Low-IF Single-chip DBS Satellite Tuner-Demodulator SoC **4:45 PM**

A. Maxim, Silicon Laboratories, Austin, TX

A fully integrated 0.13µm CMOS ring-oscillator-based PLL for low-IF single-chip DBS satellite tuner-demodulator IC is presented. A noise-attenuating loop filter reduces the oscillator gain, helping both front-end noise and spur rejection and allowing the on-chip integration of the filter capacitance. The PLL shows <1.5°$_{rms}$ double-sided integrated phase noise, <-60dBc reference spurs, <-50dBc coupled spurs. It occupies 0.3mm^2 die area and consumes 40mA at 3.3V.